ABSTRACT

A digital signal receiving system is provided for establishing high-speed clock resynchronization even if abnormality such as a poor radio wave receiving condition takes place. The system is constructed such that recipient STC data and PCR data are acquired in response to detection of a variation in frequency of a clock signal, and these data are stored as variation information data. The receiver 10 sets the PCR data in the R_STC counter 142, and sends the variation information data to the host device 20. The host device 20, in turn, sets a computation result obtained based on host STC data and the variation information data in the H_STC counter 242.